User Manual

GHD3450

Three-Phase 200V Gate Driver

Version: V1.0

Contents

1 Product Overview

1.1 Introduction

The GHD3450 is a three-phase, medium-voltage, high-speed gate driver IC. It is designed to drive dual N-channel VDMOS power transistors or IGBTs in bridge circuits. It is suitable for applications such as brushless DC motors.

The built-in dead time is typically 220ns. If the MCU output dead time is shorter than the built-in dead time, the actual dead time is the built-in dead time. If the MCU output dead time is longer than the built-in dead time, the actual dead time is the MCU output dead time. Built-in VCC and VBS undervoltage protection prevent the system from turning on external power transistors when the drive voltage is too low. The high-side and low-side driver outputs are controlled independently by their input signals.

1.2 Main Characteristics

- Supply voltage operating range: 5.5–20V
- Floating offset voltage: +200V
- Built-in dead time: 220ns (typical)
- Built-in VCC/VBS undervoltage protection
- Built-in shoot-through prevention
- Built-in input bias resistor
- Built-in output bias resistor
- Matched high-side/low-side channel propagation delay
- High dv/dt noise immunity
- Input and output are in phase
- Compatible with 3.3V/5V logic inputs
- Built-in bootstrap diode
- Peak output source current: 2.0A@15 V; fall time: 20ns with 3.3nF load
- Peak output sink current: 2.7A@15V; rise time: 35ns with 3.3nF load

1.3 Application Scope

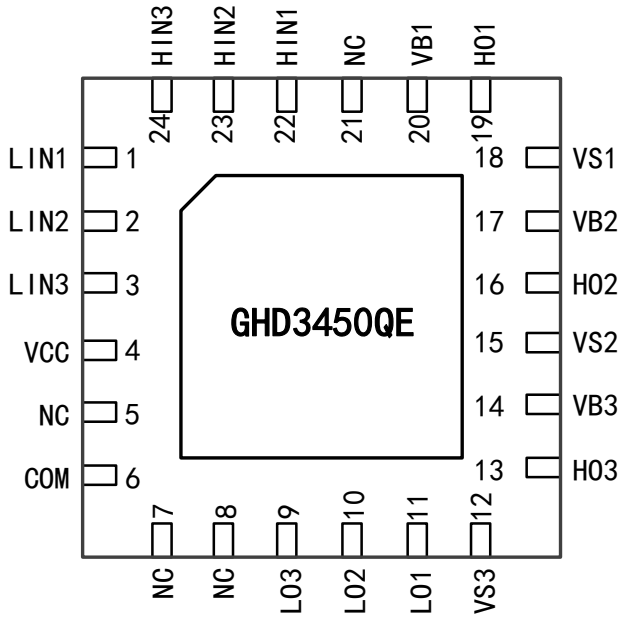
- Power Tools
- Garden Tools
- Cleaning Tools
- Drone ESCs

2 Pin Information

2.1 Pin Distribution

Figure 1 Distribution Diagram of TSSOP20 Pins

Figure 2 Distribution Diagram of QFN24 Pins



2.2 Pin Functional Description

Table 1 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviations	Definitions
Pin Name	Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name.	
Pin Type	P	Power supply pin
	I	Only input pin
	O	Only output pin
	I/O	I/O pin

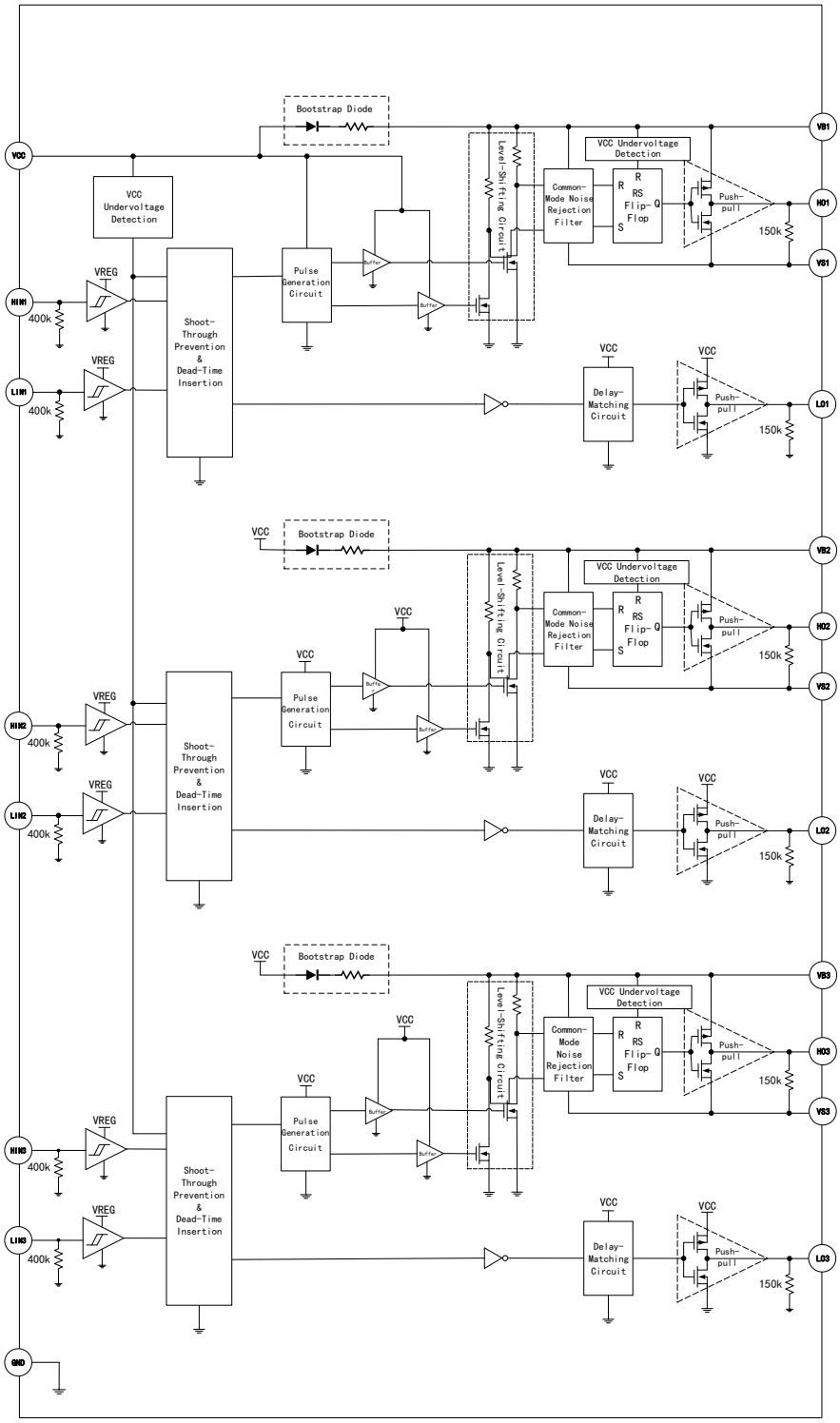
Table 2 Description of GHD3450 by Pin Number

Name	Type	Functional Description	TSSOP20 Pin Sequence	QFN24 Pin Sequence
HIN1	I	Phase-1 high-side input	1	22
HIN2	I	Phase-2 high-side input	2	23
HIN3	I	Phase-3 high-side input	3	24
LIN1	I	Phase-1 low-side input	4	1
LIN2	I	Phase-2 low-side input	5	2
LIN3	I	Phase-3 low-side input	6	3
VCC	P	Chip drive power supply pin	7	4
GND	P	Chip signal ground pin	8	6
LO3	O	Phase-3 low-side output	9	9
LO2	O	Phase-2 low-side output	10	10
LO1	O	Phase-1 low-side output	11	11
VS3	P	Phase-3 high-side floating pin	12	12
HO3	O	Phase-3 high-side output	13	13
VB3	P	Phase-3 high-side bootstrap power pin	14	14
VS2	P	Phase-2 high-side floating pin	15	15
HO2	O	Phase-2 high-side output	16	16
VB2	P	Phase-2 high-side bootstrap power pin	17	17
VS1	P	Phase-1 high-side floating pin	18	18
HO1	O	Phase-1 high-side output	19	19
VB1	P	Phase-1 high-side bootstrap power pin	20	20
NC	-	-	-	5,7,8,21

3 Block Diagram Logic

3.1 Internal Block Diagram

Figure 3 GHD3450 Internal Block Diagram



3.2 Logic Truth Value

Table 3 Logic Truth Value

VCCUV	VBSUV	LIN	HIN	LO	HO
normal	normal	L	H	L	H
normal	normal	H	L	H	L
normal	normal	L	L	L	L
normal	normal	H	H	L	L
normal	UV	H&L	H&L	H&L	L
UV	normal	H&L	H&L	L	L

Note:

(1) VBS undervoltage will only set the HO output low.

(2) VCC undervoltage will set both LO and HO outputs low.

4 Electrical Characteristics

4.1 Recommended Safe Operating Range

Unless otherwise specified, T_A = 25 °C and all pins are referenced to GND.

Table 4 General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	-	105	℃
$V_{HO1,2,3}$	High-side output voltage	$VS_{1,2,3}$	$VS_{1,2,3}$+15	$VB_{1,2,3}$	V
$V_{LO1,2,3}$	Low-side output voltage	0	15	VCC	V
$VB_{1,2,3}$	High-side floating offset absolute voltage	$VS_{1,2,3}$+5.5	$VS_{1,2,3}$+15	$VS_{1,2,3}$+20	V
$VS_{1,2,3}$	High-side floating offset relative voltage	-5	-	140	V
VCC	Supply voltage	5.5	15	20	V
V_{IN}	Input voltage (HIN1, 2, 3/LIN1, 2, 3)	0	-	5	V

Note:

(1) When $VB_{1, 2,3}$=$VS_{1, 2,3}$+10, VS =（GND-5V）~（GND-VBS）, HO holds its logic state , if （GND-5V）< $VS_{1, 2,3}$< 40V, HO operates normally.

(2) Operation beyond the recommended conditions for a long time may affect its reliability.

4.2 Absolute Maximum Rated Value

Unless otherwise specified, T_A = 25 °C and all pins are referenced to GND.

Table 5 Power Consumption

Symbol	Description	Min	Max	Unit
P_D	Maximum power consumption	-	1.25	W

Note: Power dissipation must never exceed P_D. The maximum power dissipation at different ambient temperatures is calculated as: P_D = 150 °C − T_A / θ_{JA}, where 150 °C is the maximum operating junction temperature, T_A is the operating ambient temperature, and θ_{JA} is the package thermal resistance.

Table 6 Temperature Characteristics

Symbol	Description	Min	Max	Unit
T_s	Storage temperature	-55	150	℃
θ_{JA}	Junction-to-ambient thermal resistance	-	100	℃/W
T_J	Junction temperature	-	150	℃
T_L	Pin welding temperature (duration 10s)	-	260	℃

Table 7 Maximum Rated Voltage Characteristics

Symbol	Description	Min	Max	Unit
$V_{HO1,2,3}$	High-side output voltage	$VS_{1,2,3}$-0.3	$VB_{1,2,3}$+0.3	V
$V_{LO1,2,3}$	Low-side output voltage	-0.3	VCC+0.3	V
$VB_{1,2,3}$	High-side floating offset absolute voltage	-0.3	225	V
$VS_{1,2,3}$	High-side floating offset relative voltage	$VB_{1,2,3}$-25	$VB_{1,2,3}$+0.3	V
VCC	Maximum supply voltage	-0.3	25	V
V_{IN}	Maximum input voltage (HIN1,2,3/LIN1,2,3)	-0.3	12	V
dVS/dt	Maximum slew rate of offset voltage	-	50	V/ns

Table 8 ESD Characteristics

Symbol	Description	Min	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	-	1000	V

Note: The 100pF capacitor is discharged through a 1.5kΩ resistor.

4.3 Electrical Characteristic Parameters

Unless otherwise specified, T_A = 25 °C, VCC = $VB_{S1,2,3}$ = 15V, $VS_{1,2,3}$ = GND, and all pins are referenced to GND.

Table 9 Supply Current Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CCQ}	VCC quiescent current	V_{IN}=0V	290	320	490	μA
I_{BSQ}	VBS quiescent current	V_{HIN}=0V, I_{BSQ1}+ I_{BSQ2}+ I_{BSQ3}	80	110	140	μA
I_{CCD}	VCC dynamic current	f_{LIN}=20kHz	750	820	940	μA
I_{BSD}	VBS dynamic current	f_{HIN}=20kHz, I_{BSD1}+ I_{BSD2}+ I_{BSD3}	310	390	680	μA
I_{LK}	VB floating power supply leakage current	V_{IN}=float,VB=225V	-	-	10	μA

Table 10 Supply Voltage Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC_{HY+}	VCC undervoltage high-level potential		3.5	4.5	5.4	V
VCC_{HY-}	VCC undervoltage low-level potential		3.4	4.3	5.2	V
VCC_{HY}	VCC undervoltage hysteresis level		-	0.2	-	V
VBS_{HY+}	VBS undervoltage high-level potential		3.2	4.2	5.0	V
VBS_{HY-}	VBS undervoltage low-level potential		3.1	4.0	4.9	V
VBS_{HY}	VBS undervoltage hysteresis level		-	0.2	-	V
VS_{QN}	VS static negative voltage	VBS=15V	-5	-	-	V

Table 11 Input-end Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN+}	Input high-level potential		1.6	2.0	2.3	V
V_{IN-}	Input low-level potential		0.8	1.7	2.1	V
V_{INHY}	Input hysteresis level		-	0.3	-	V
I_{IN+}	Input high-level current	V_{HIN}=5V, V_{LIN}=0V	9	13	19	μA
I_{IN-}	Input low-level current	V_{HIN}=0V, V_{LIN}=5V	-	-	1	μA

Table 12 Driver output-end Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OUT+}	High-level output voltage	I_{OUT}=100mA, 15V- V_{OUT}	220	330	800	mV
V_{OUT-}	Low-level output voltage	I_{OUT}=100mA, V_{OUT}-GND	80	140	300	mV
V_{OUT+}	Low-level output voltage	I_{OUT}=20mA, 15V- V_{OUT}	60	70	150	mV
V_{OUT-}	Low-level output voltage	I_{OUT}=20mA, V_{OUT}-GND	15	30	60	mV
I_{OUT+}	High-level short-circuit pulse current	V_{IN}=5V V_O=0V PWD≤10μs	1.6	2.0	3.0	A
I_{OUT-}	Low-level short-circuit pulse current	V_{IN}=0V V_O=15V PWD≤10μs	2.0	2.7	3.2	A

Table 13 Time Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{ON}	Output rising edge transmission time	No Load	130	170	250	ns
T_{OFF}	Output falling edge transmission time	No Load	130	170	250	ns
T_R	Output rise time	C_L=3.3nF	20	35	60	ns
T_F	Output fall time	C_L=3.3nF	15	20	40	ns
DT	Dead time	No Load	160	220	300	ns
MT	High and low-side matching time	No Load	-	-	30	ns

Table 14 Bootstrap Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{BSD15L}	Bootstrap charging current	VCC=15V VB=11V	10	15	25	mA
I_{BSD15H}	Bootstrap charging current	VCC=15V VB=0V	60	85	110	mA

5 Description of Application

5.1 Recommended Application Circuit Diagram

Figure 4 Application Circuit

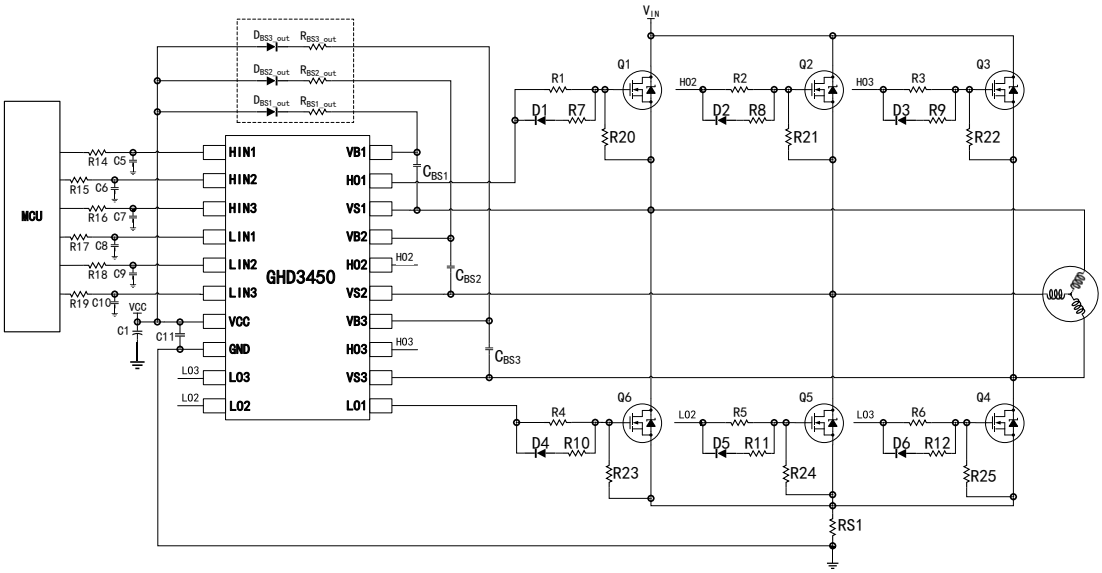


Table 15 Recommended Parameters

Designation	Name	Typical Application Value	Recommended Package
C1	Power energy-storage capacitor	100μF/50V	Electrolytic capacitor
C11	Power filter capacitor	1uF/50V	SMD capacitor 1206
R14, R15, R16, R17, R18, R19	Input filter resistor	100Ω/5%	SMD resistor 0603
C5, C6, C7, C8, C9, C10	Input filter capacitor	100pF	SMD capacitor 0603
R1, R2, R3, R4, R5, R6	Output drive resistor	30Ω/1%, application-dependent	SMD resistor 0603
R7, R8, R9, R10, R11, R12	Fast turn-off resistor	30Ω/1%, application-dependent	SMD resistor 0603
D1, D2, D3, D4, D5, D6	Fast turn-off diode	1N4148	SOD323
R20, R21, R22, R23, R24, R25	Gate pull-down resistor	100kΩ	SMD resistor 0805
D_{BS1_OUT}, D_{BS2_OUT}, D_{BS3_OUT}	Bootstrap diode	Select reverse breakdown voltage > 225V	SMB

Designation	Name	Typical Application Value	Recommended Package
R_{BS1_OUT}, R_{BS2_OUT}, R_{BS3_OUT}	Bootstrap current-limiting resistor	10Ω	SMD resistor 0805
C_{BS1}, C_{BS2}, C_{BS3}	Bootstrap energy-storage capacitor	10uF/50V	SMD capacitor 1206
Q1, Q2, Q3, Q4, Q5, Q6	Power transistors	Based on the application	-
RS1	Bus current sense resistor	Based on the application	-

Notes:

(1) The power energy-storage capacitor C1 requires a high capacitance to keep the supply stable.

(2) The power filter capacitor C11 has a lower capacitance than C1 and filters the supply noise.

(3) Choose output drive resistors R_1–R_6 based on the driven device, dead time, MOSFET power dissipation, and EMC requirements. A reverse-diode fast turn-off circuit or PNP-transistor fast turn-off circuit is recommended.

(4) R_{14}–R_{19} and C_5–C_{10} form the input RC filter circuit and reduce signal noise.

(5) For bootstrap capacitors CBS1–CBS3, select a voltage rating above 2 × VCC and a capacitance from 1μF to 100μF. It is best to choose the value based on the measured ripple. A clamping diode is recommended.

(6) R_7–R_{12} and D_1–D_6 form the fast turn-off circuit. This increases turn-off speed and reduces parasitic conduction.

(7) For bootstrap diodes $D_{BS1\_OUT–DBS3\_OUT}$, fast-recovery diodes are recommended. Select a voltage rating above 1.5 × VIN and an instantaneous current rating greater than 1 A. Use a current-limiting resistor and choose the parts based on the actual power-up and charging time.

5.2 PCB Layout Suggestions

(1) Place the chip supply filter capacitors C11 close to the chip, between the VCC and GND pins. Place the bootstrap current-limiting resistors $R_{BS1–3\_OUT}$, bootstrap diodes $D_{BS1–3\_OUT}$, and bootstrap capacitors C_{BS} close to the related chip pins. Keep the loop area as small as possible.

(2) Keep the trace length between the PWM output and the chip PWM input as short as possible. Place filter resistors/capacitors R_{14}–R_{19} and C_5–C_{10} close to the chip pins.

(3) Place output drive resistors R_1–R_6 and fast turn-off resistors R_7–R_{12} close to the gates of Q1–Q6. This reduces drive-signal oscillation caused by trace inductance.

(4) Keep the power loop area as small as possible. Route power ground, supply ground, and signal ground separately.

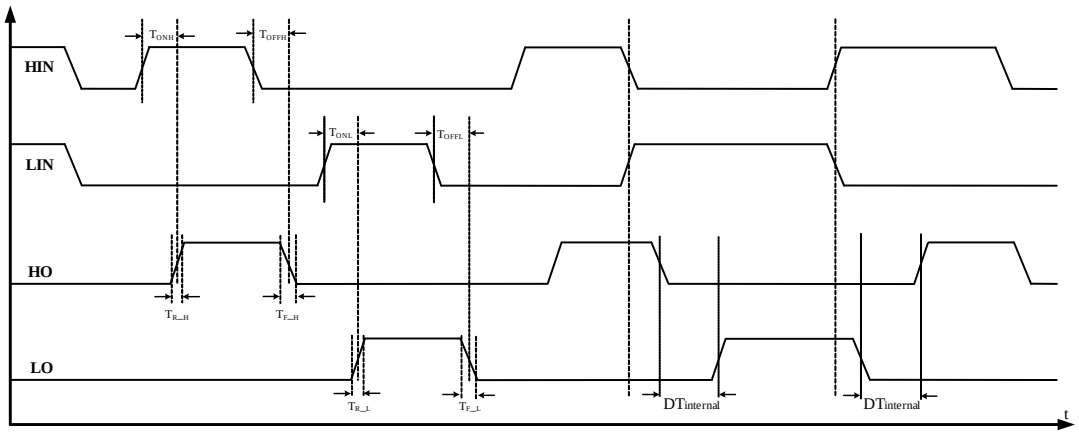
(5) If the circuit uses a DC-DC switching power supply, keep the DC-DC loop area as small as possible because it operates at high frequency. Follow the layout recommendations for the specific DC-DC chip used.

6 Test instructions

6.1 Time Parameter Test

Timing parameters mainly include output rise time T_R, output fall time T_F, rising-edge propagation delay T_{ON}, falling-edge propagation delay T_{OFF}, and dead time DT.

Figure 5 Time Parameters



6.2 VCC and VBS Undervoltage Test

VCC is the low-side supply, and VBS is the high-side supply.

To prevent the system from turning on external power transistors at low drive voltages, the chip includes an undervoltage lockout circuit. The VCC undervoltage high and low thresholds are level-triggered. The VBS undervoltage high threshold is edge-triggered and requires an HIN edge to retrigger. The VBS undervoltage low threshold is level-triggered.

Figure 6 VCC Undervoltage Timing Diagram (Ignoring Transmission Delay)

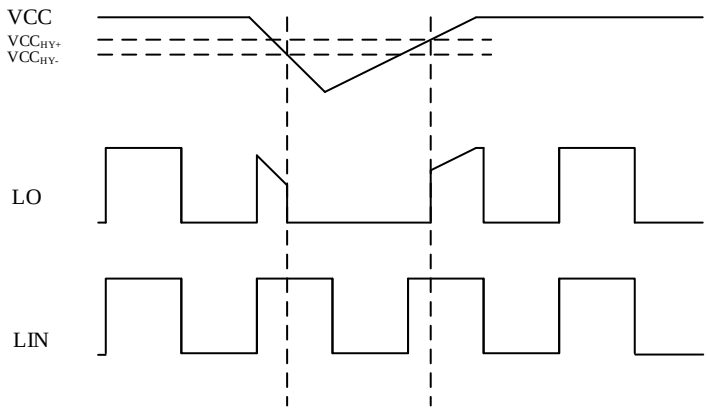
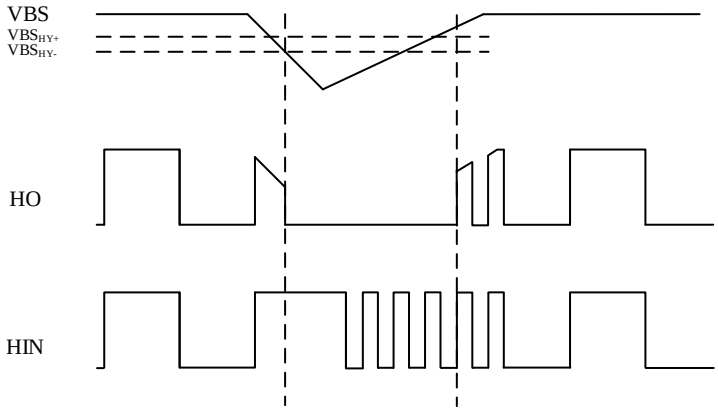


Figure 7 VBS Undervoltage Timing Diagram (Ignoring Transmission Delay)

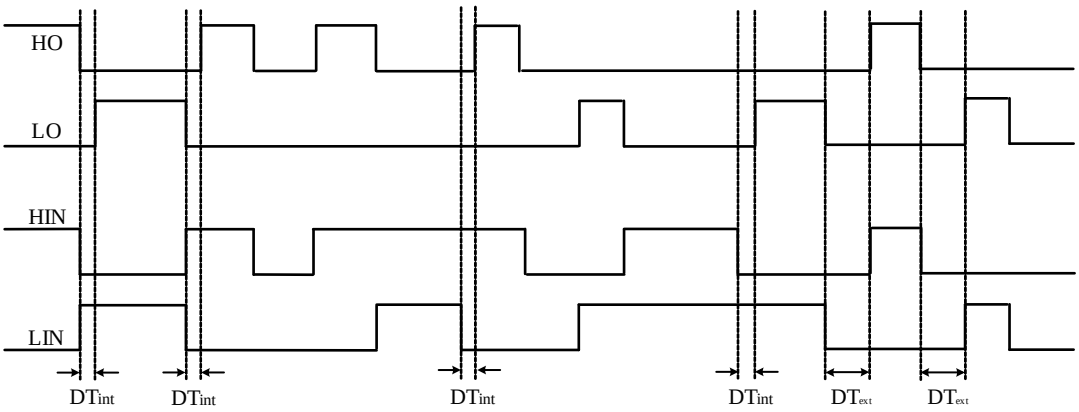


6.3 Shoot-Through Protection and Dead-Time Test

The chip includes built-in shoot-through protection and dead-time protection based on the input signals. When both inputs are high, the chip identifies the state as a shoot-through condition, and the corresponding outputs are pulled low. Under all input conditions, at least one dead-time interval is inserted between output high levels. The relationship between the external input-side dead time DT_{ext} and the built-in dead time DT_{int} is as follows:

- If $DT_{ext}>DT_{int}$, $DT=DT_{ext}$
- If $DT_{ext}<DT_{int}$, $DT=DT_{int}$

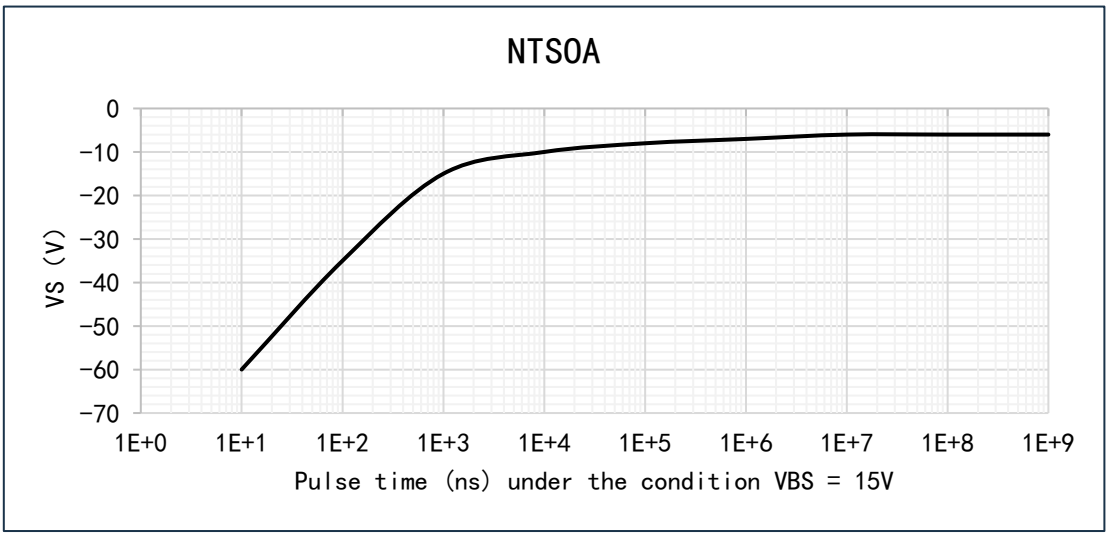
Figure 8 Logic Timing Diagram (Ignoring Transmission Delay)



6.4 Negative Transient Safe Operating Area

The Negative Transient Safe Operating Area, or NTSOA, describes the gate driver's ability to withstand transient negative voltages. For negative pulses above the NTSOA boundary, the gate driver can usually avoid failure. In practice, a sufficient design margin is recommended. Negative pulses below the NTSOA boundary may cause abnormal operation or permanent damage.

Figure 9 Negative Transient Safe Operating Area



7 Package Information

7.1 TSSOP20 Package Diagram

Figure 10 TSSOP20 Package Diagram

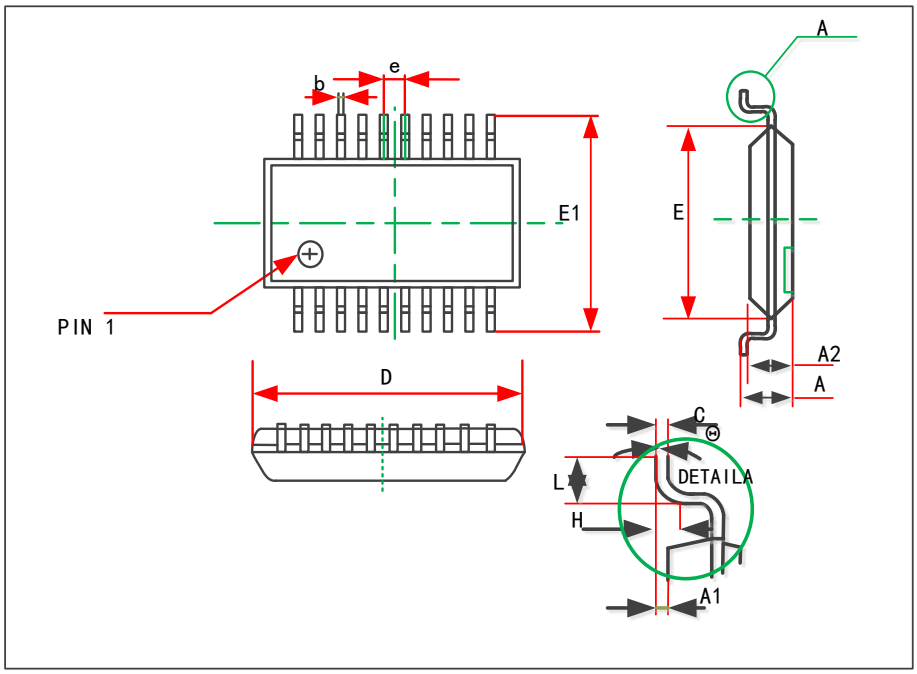


Table 16 TSSOP20 Package Parameter

SYMBOL	Dimensions IN Millimeters		Dimensions IN Inches	
	MIN	MAX	MIN	MAX
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	-	1.200	-	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	

Note:

(1) Dimensions are marked in millimeters.

(2) BSC is a unit without error, which refers to millimeter here.

Figure 11 TSSOP20 Soldering Layout Recommendation

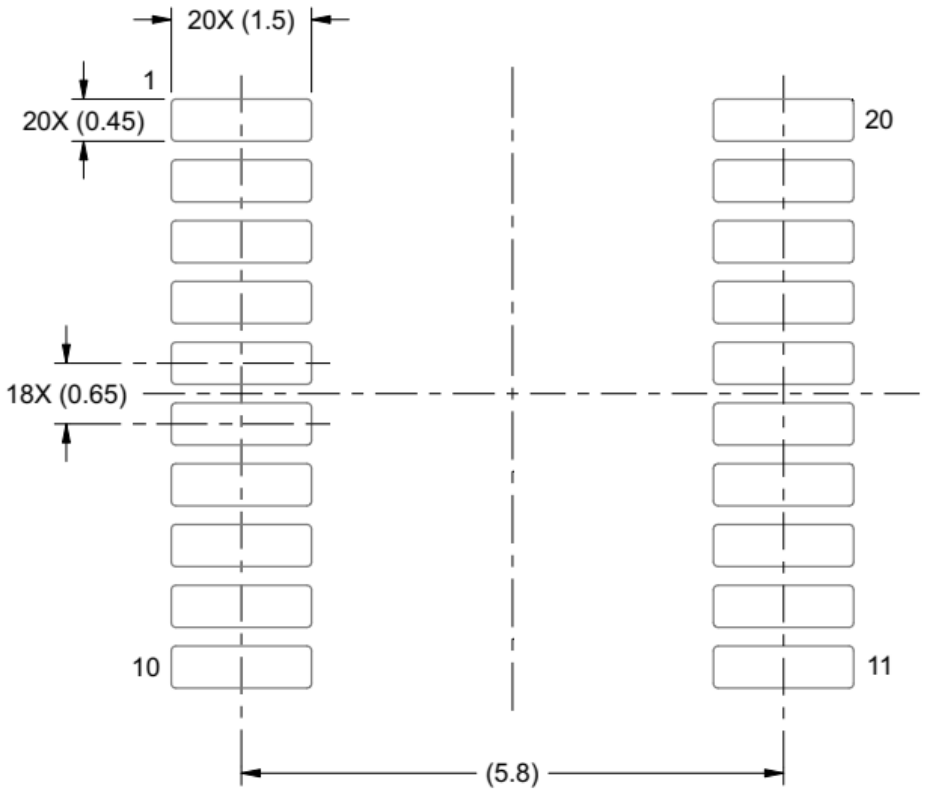
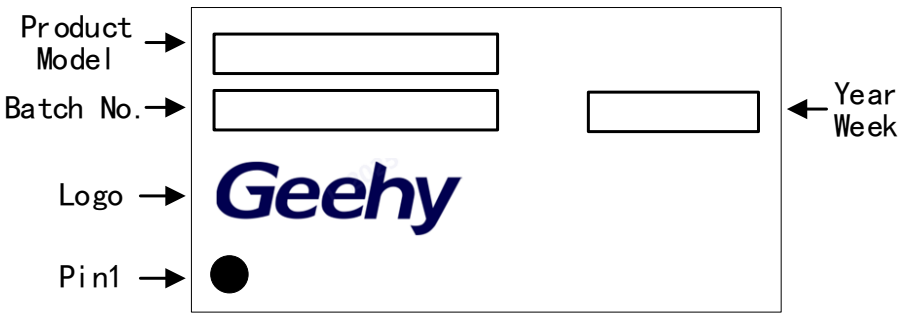
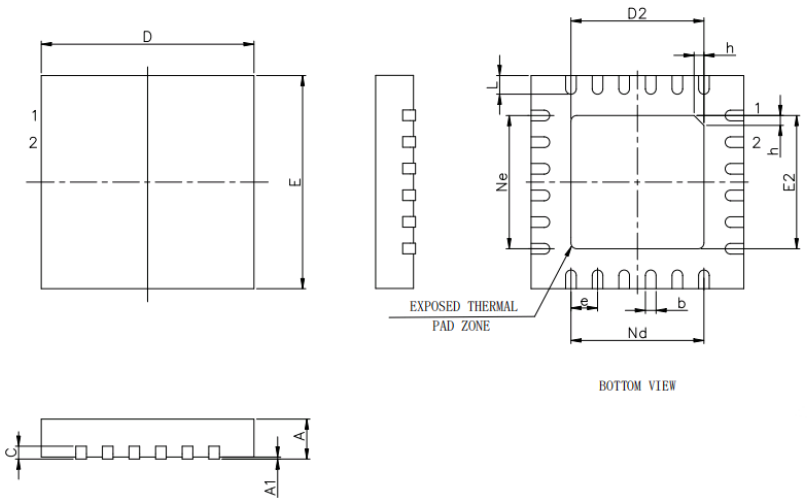


Figure 12 TSSOP20 Package Identification



7.2 QFN24 Package Diagram

Figure 13 QFN24 Package Diagram



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 14 QFN24 Soldering Layout Recommendation

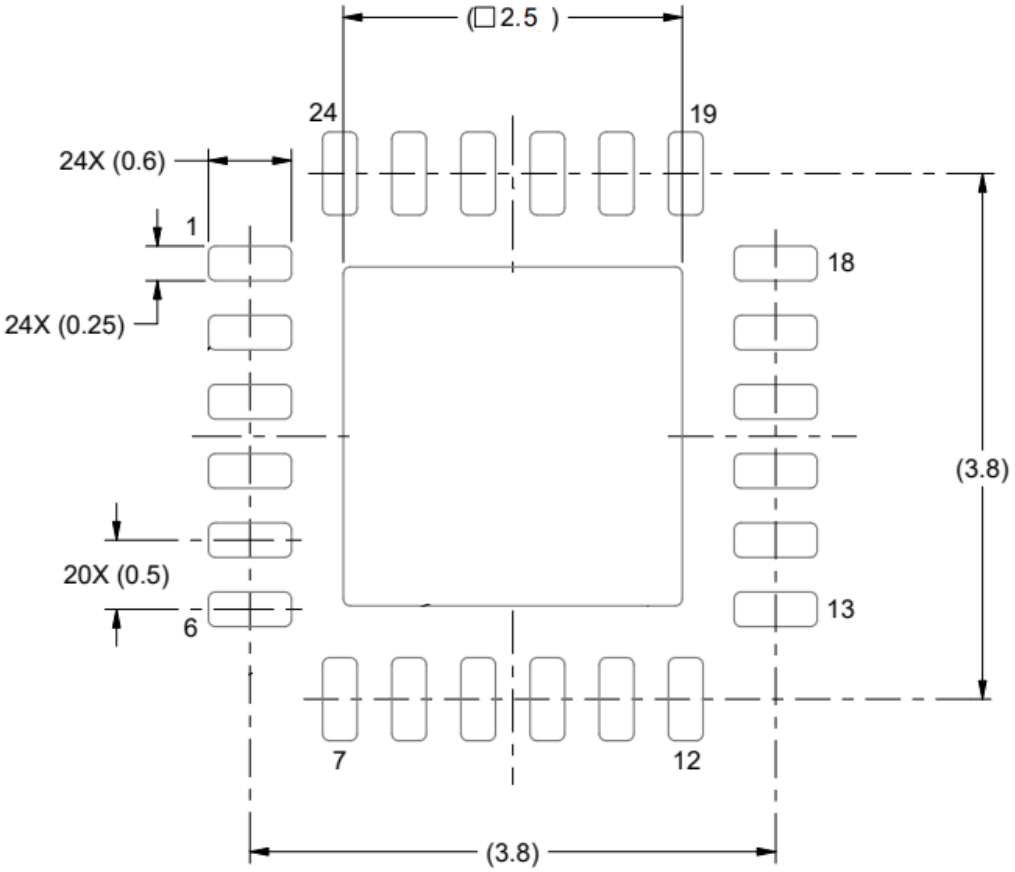
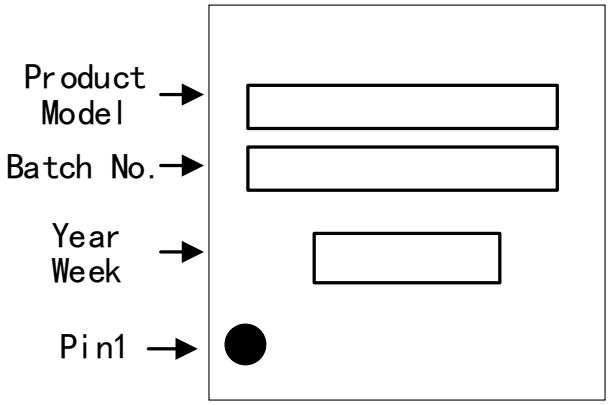


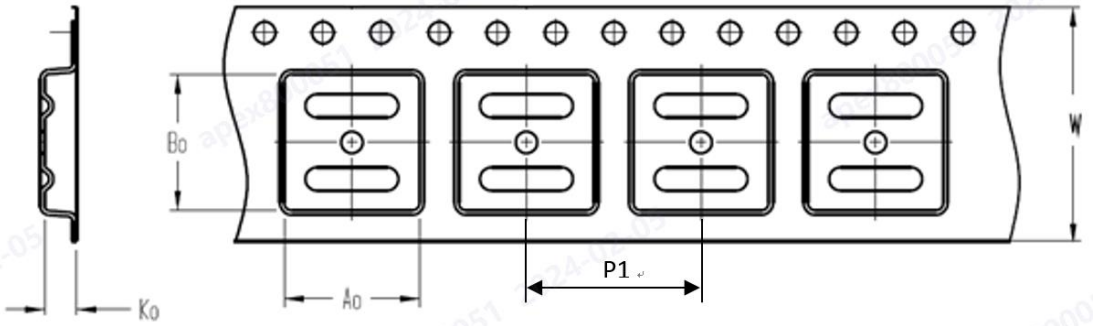
Figure 15 QFN24 Package Identification



8 Packaging Information

8.1 Reel Packaging

Figure 1Tape Dimensions



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
P1	Dimension designed to accommodate the component pitch
W	Overall width of the carrier tape

Figure 2 Quadrant allocation in PIN1 direction in tape

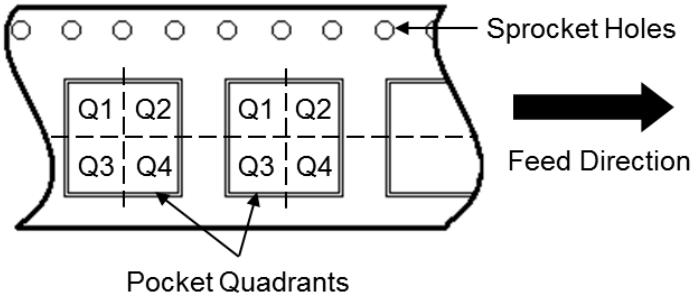


Figure 3 Reel Dimensions

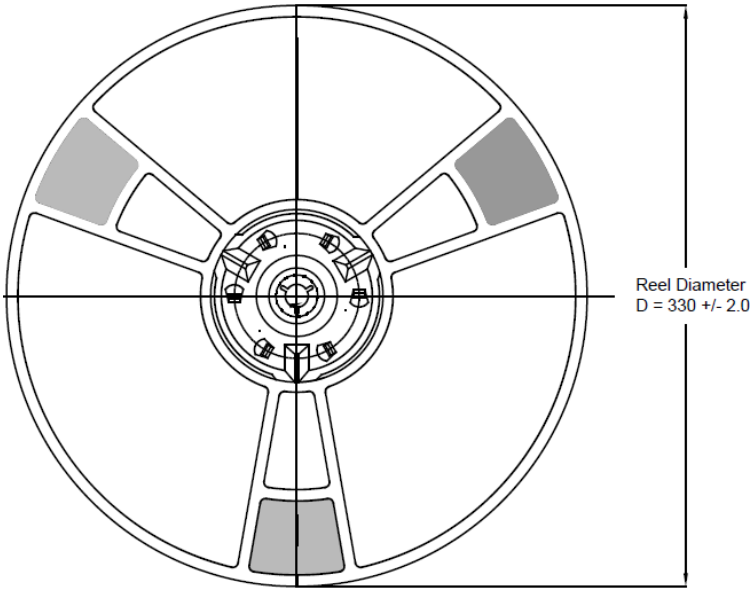
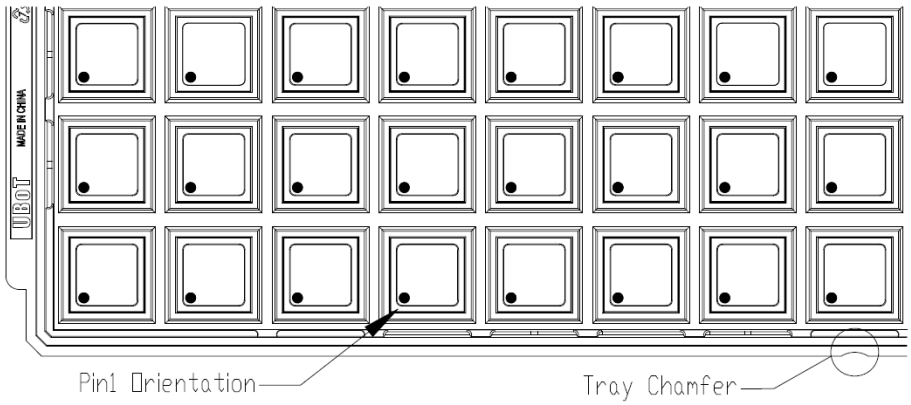


Table 17 Tape packaging parameter specification table

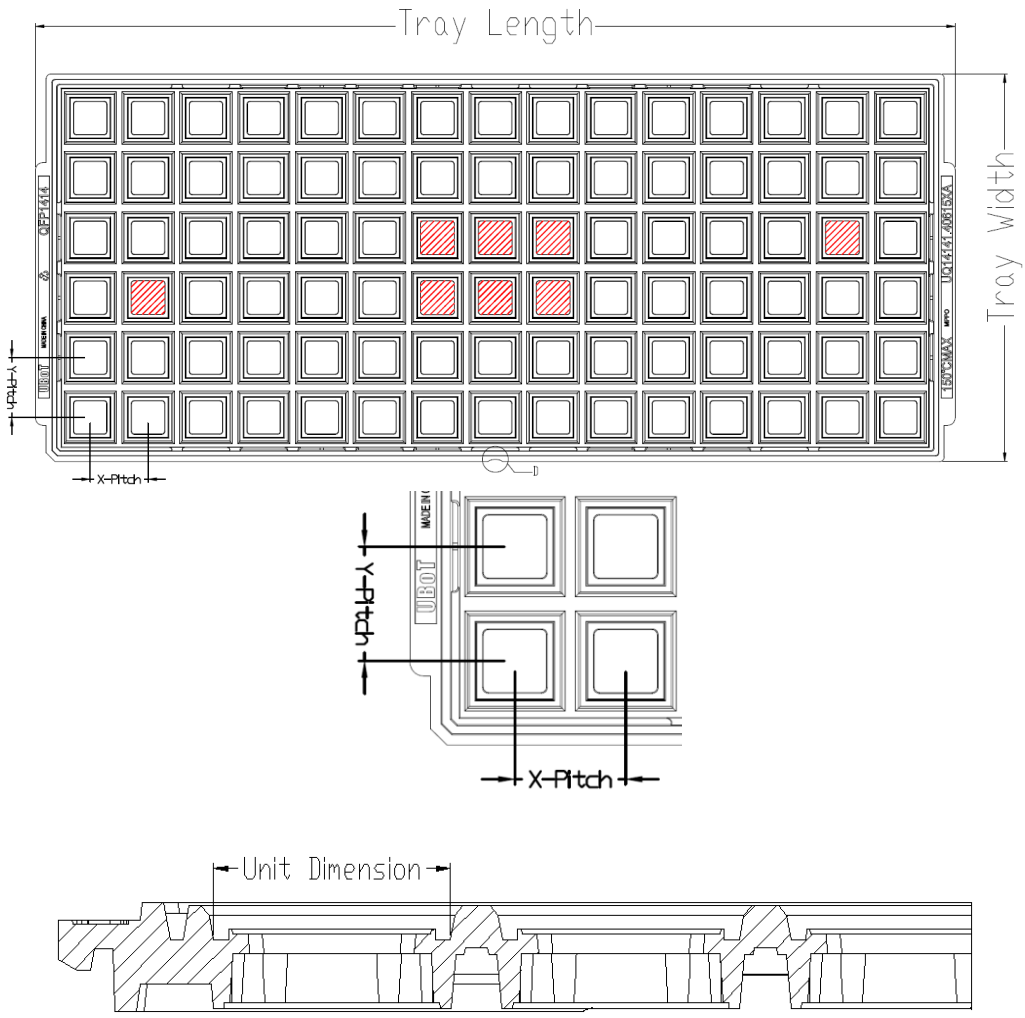
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	P1 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
GHD3450PF	TSSOP	20	4000	330	6.8	6.95	8	1.5	16	Q1
GHD3450QE	QFN	24	5000	330	4.3	4.3	8	1.1	12	Q1

8.2 Tray packaging

Figure 4 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product

Table 18 Tray Packaging Parameter Specification Table

Device	PKG Type	Pins	SPQ	X-Dimension	Y-Dimension	X-Pitch	Y-Pitch	Tray Length	Tray Width
GHD3440QE	QFN	20	4900	4.2	4.2	8.8	9.2	322.6	135.9

9 Ordering Information

Table 19 Ordering Information

Device	Package	Packaging	SPQ
GHD3450PF	TSSOP20	Reel	4000
GHD3450QE	QFN24	Reel	5000
GHD3450QE	QFN24	Tray	4900

10 Revision History

Table 20 Document Revision History

Date	Version	Revision History
2026.8	1.0	● Initial release

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